an interface connected to exchange data and addresses with an external system,

a data buffer connected to exchange data between the flash memory and the interface,

addressing circuits responsive to a sector address received through the external system interface to (a) address a corresponding block, (b) read the block address stored in the block address area of said corresponding block, and (c) if the read block address is not the address of said corresponding block, addressing another block having the address read from said corresponding block.

67. The semiconductor disk device of claim 66, wherein the flash memory includes an array of EEPROM cells that are individually programmable into exactly two states in order to store one bit of data per cell.

68. The semiconductor disk device of claim 66, wherein the flash memory includes an array of EEPROM cells that are individually programmable into more than two states in order to store more than one bit of data per cell.

69. In memory system that includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, a method of operating the memory system with a host computer, comprising:

configuring use of the memory cells within the individual sectors to provide at least distinct portions in which user data and a sector address are stored,

in response to receiving a memory address from the host computer, addressing a corresponding sector and reading the sector address from the sector address portion thereof,

if the read sector address is that of the addressed corresponding sector, sending data to the host computer that is read from the user data portion of the addressed corresponding sector, and

if the read sector address is that of a sector other than the addressed corresponding sector, addressing the other sector and sending data to the host computer that is read from the user data portion of the other sector.

70. The method of claim 69, wherein the memory array is operated with the individual cells thereof being programmable into one of exactly two detectable states in order to store one bit of data per cell.

71. The method of claim 69, wherein the memory array is operated with the individual cells thereof being programmable into one of more than two detectable states in order to store more than one bit of data per cell.

72. The method of any one of claims 69-71, additionally comprising providing the memory array within a card that is removably connectable to the host computer system.

73. The method of any one of claims 69-71, wherein the user data portion of the individual memory sectors has a capacity of 512 bytes of data.--

REMARKS

By this Preliminary Amendment, the original parent application claims are being canceled and a new set of claims being substituted. New claims 63-65 are substantial copies of claims 1 and 2 of U.S. patent no. 5,627,783 - Miyauchi (1997). New claims 66-73 are directed to similar subject matter.

Dependent claims 68 and 71 are directed to multi-state operation of the flash EEPROM cells, wherein more than one bit of data is stored in each cell. Although multi-state operation is mentioned in the present application specification, it is more completely discussed in two applications incorporated by reference into the specification at pages 11, 22 and 26. Since the referenced application serial no. 204,175 has issued as patent no. 5,095,344, the patent number is being added by this Amendment. The serial number of the second referenced application is also being added by this Amendment. The status of the second referenced application is that it has become abandoned in favor of a continuation-in-part application which matured into patent no. 5,172,338 and a division thereof into patent no. 5,163,021. Copies of the 4 patents referenced in these Remarks are being filed with this Amendment, for the convenience of the Examiner.